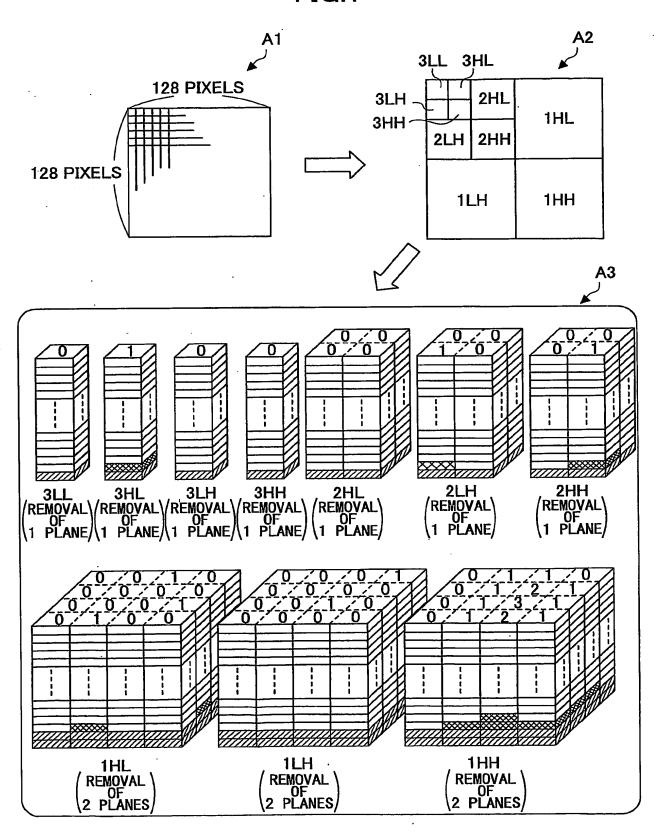
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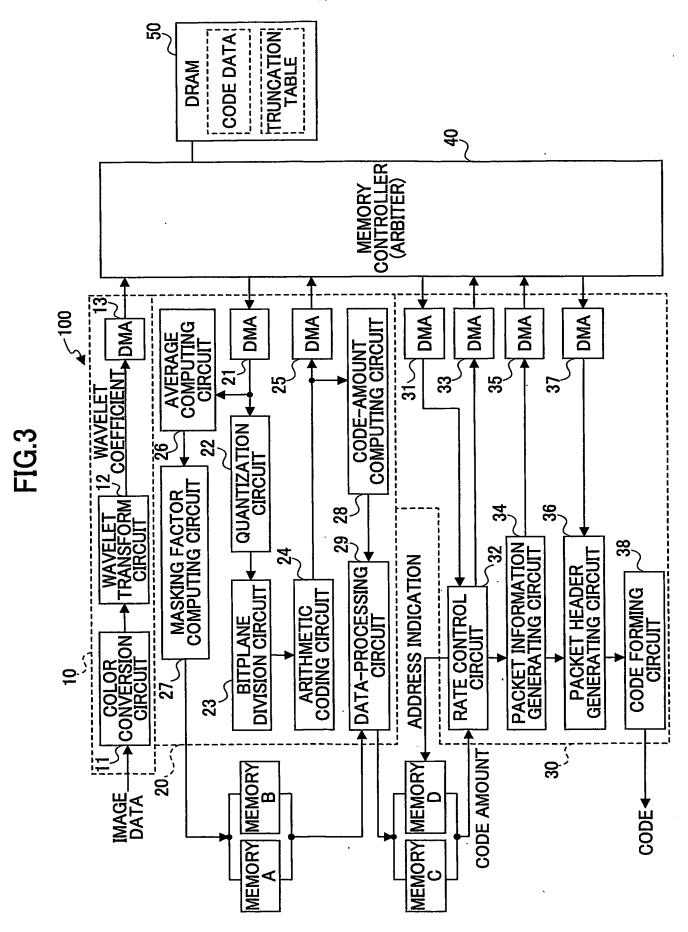
FIG.1



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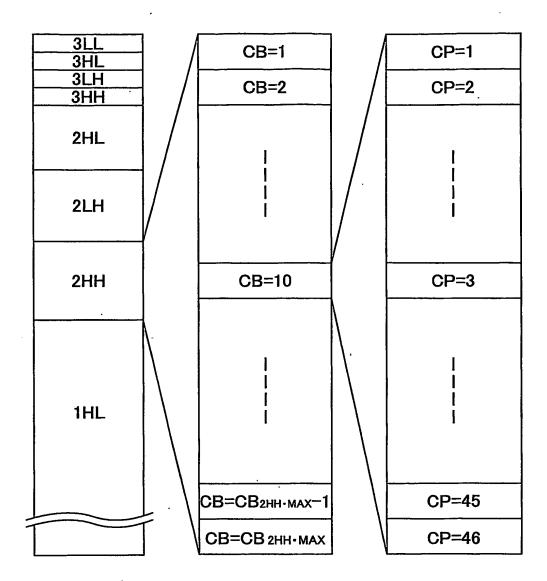
	V 211 201 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	V 211 201 -1 U-UU
DATA No. T	Y 3LL, 3HL-LH-HH, 2HL-LH-HH, 1HL-LH-HH Cb 3LL, 3HL-LH-HH 2HL-LH-HH, 1HL-LH-HH Cr 3LL, 3HL-LH-HH 2HL-LH-HH, 1HL-LH-HH	Y 3LL, 3HL-LH-HH, 2HL-LH-HH, 1HL-LH-HH Cb 3LL, 3HL-LH-HH 2HL-LH-HH, 1HL-LH-HH Cr 3LL, 3HL-LH-HH 2HL-LH-HH, 1HL-LH-HH
T=0	0, 0 0 0, 0 0 0, 0 0 0 0, 0 0 0, 0 0 0, 0 0 1 0, 0 0 0, 0 0 0, 0 0	T=399 1, 1 1 3, 4 4 6, 101017 9, 101013, 141418, 202027 8, 9 911, 121216, 181823
T=1	0, 0 0 0, 0 0 0, 0 0 0 0, 0 0 0, 0 0 0, 0 0 2 0, 0 0 0, 0 0 0, 0 0	T=400 1, 1 1 3, 4 4 6, 101017 9, 101013, 141418, 202027 8, 9 911, 121216, 181823
T=2	0, 0 0 0, 0 0 0, 0 0 0 0, 0 0 0, 0 0 0, 0 0 3 0, 0 0 0, 0 0 0, 0 0	
	•	T=499
T=99	0, 0 0 0, 0 0 0, 0 0 6 0, 0 0 3, 4 4 8, 101017 0, 0 0 1, 2 2 6, 7 713	T=500
T=100	0, 0 0 0, 0 0 0, 0 0 7 0, 0 0 3, 4 4 8, 101017 0, 0 0 1, 2 2 6, 7 713	•
	•	T=1000
T=199	0, 0 0 0, 0 0 0, 5 511 3, 4 4 7, 8 813, 151521 2, 3 3 6, 7 710, 121217	•
T=200	0, 0 0 0, 0 0 0, 5 511 3, 4 4 7, 8 813, 151522 2, 3 3 6, 7 710, 121217	T=1500
•	•	
T=299	0, 0 0 0, 1 1 4, 8 814 6, 7 710, 111216, 181825 6, 6 6 9, 101013, 151520	
T=300	0, 0 0 0, 1 1 4, 8 814 6, 7 710, 121216, 181825 6, 6 6 9, 101013, 151520	
	•	



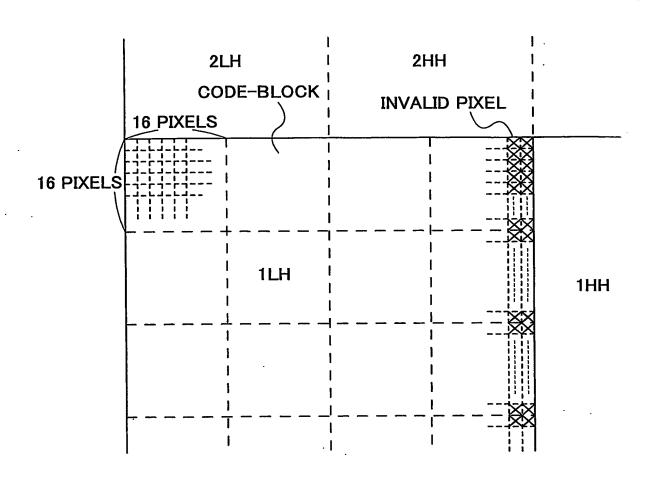


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6/18 **FIG.6**

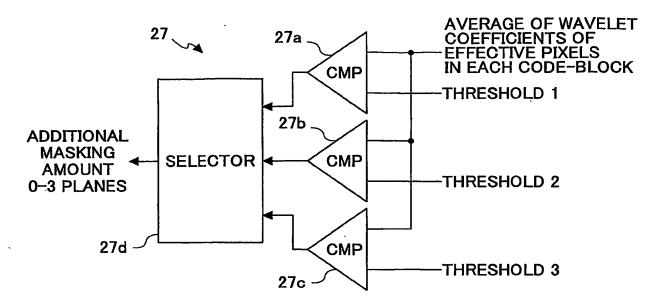
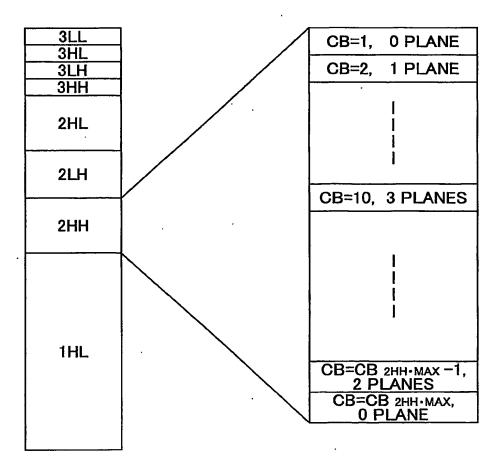
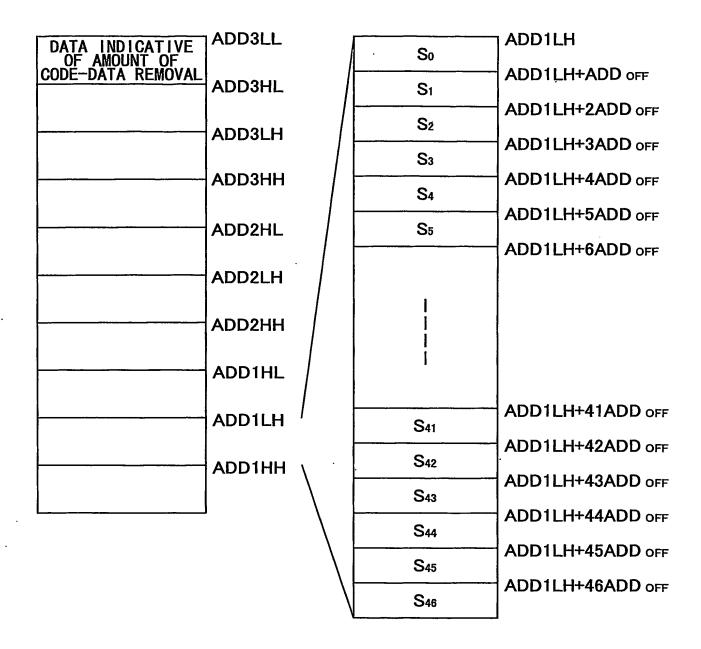


FIG.7



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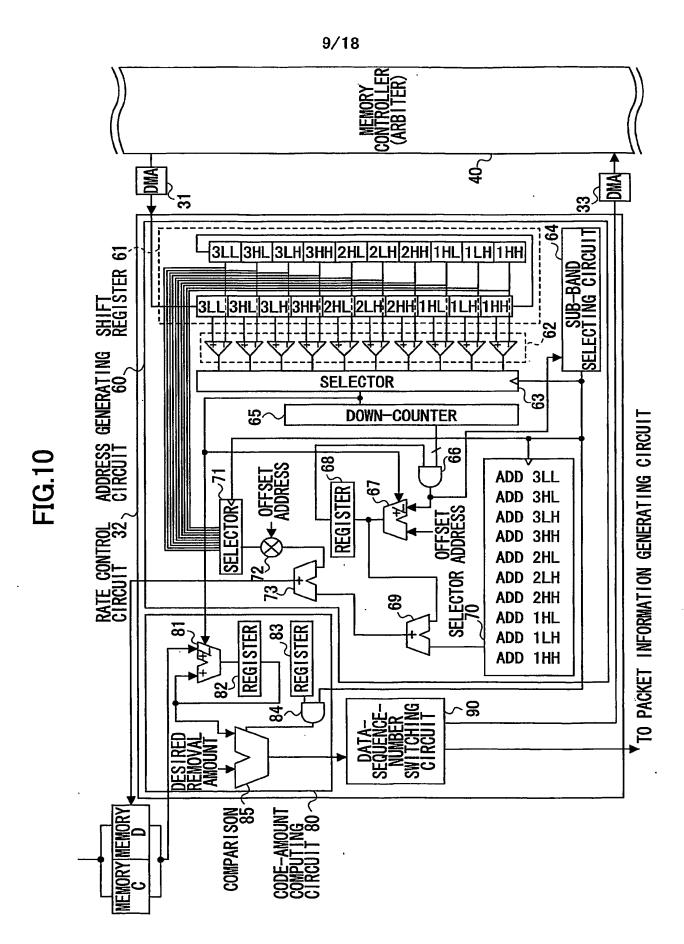
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8/18 FIG.9 START SB=1 S1 ~ BP=0, S_{BP}=0 S3 / CB=1 Q=BP+M(CB) S5> COMPUTE TOTAL AMOUNT SBP (CB) OF CODING-PASS CODES, WHICH IS EQUAL IN AMOUNT TO Q PLANES FROM THE LOWEST-ORDER BITPLANE IN CODE-BLOCK IDENTIFIED BY CB NO BP≧1 **S7**> ¥YES COMPUTE DIFFERENCE FROM PRECEDING TOTAL CODE AMOUNT SBP(CB)=SBP(CB)-SBP-1(CB). S8^ SBP=SBP+SBP(CB) CB=CB+1 NO CB>CBsB·MAX **S10** S115 YES STORE CODE AMOUNT SBP AT ADDRESS ADD"SB" + OFFSET ADDRESS ADD $^{\circ}$ SFXBP BP=BP+1 S12/ NO BP>46 **S13 ¥YES** SB=SB+1 S14 NO SB>10

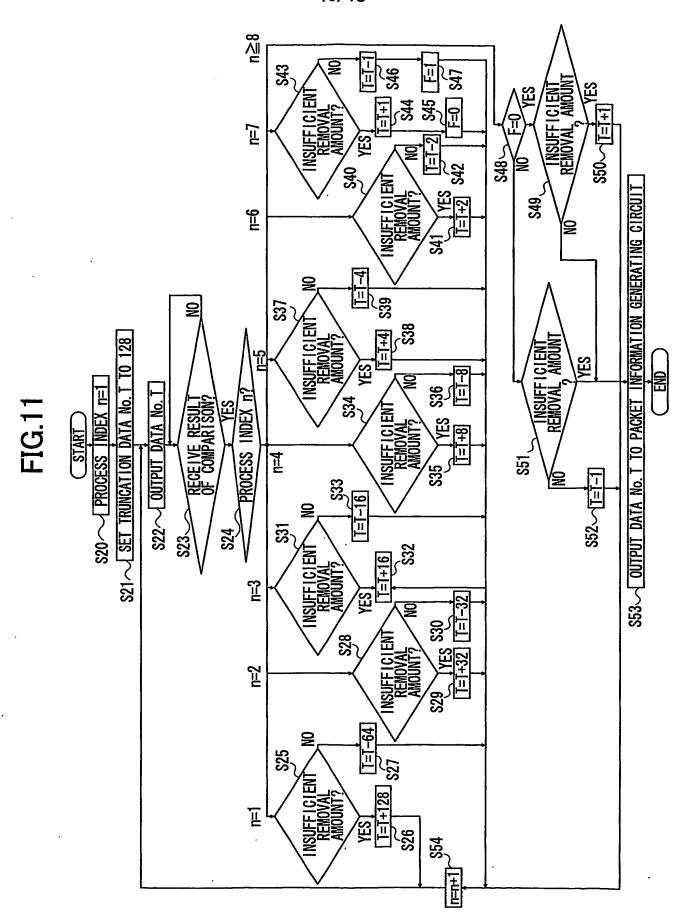
¥YES

END

S15

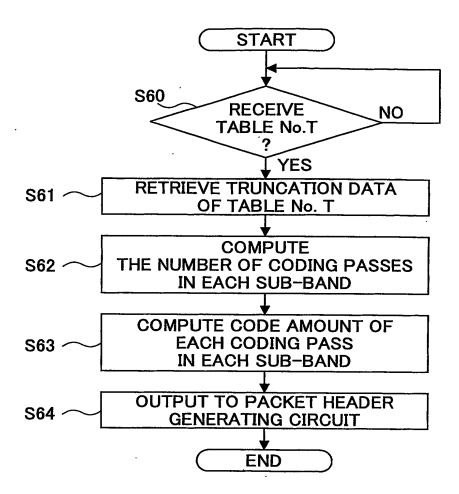


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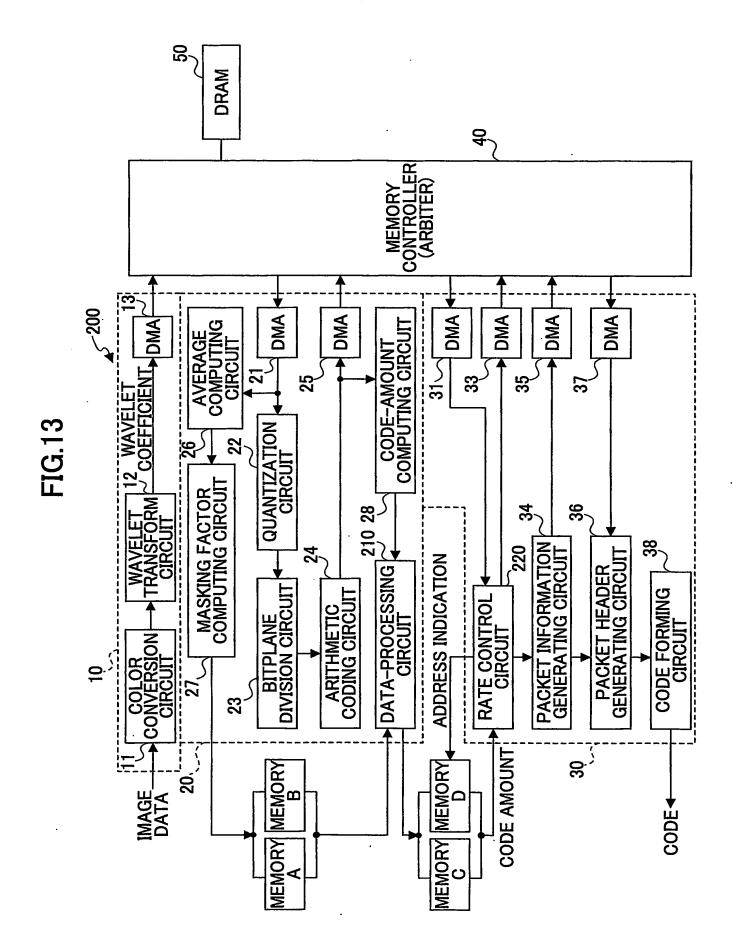


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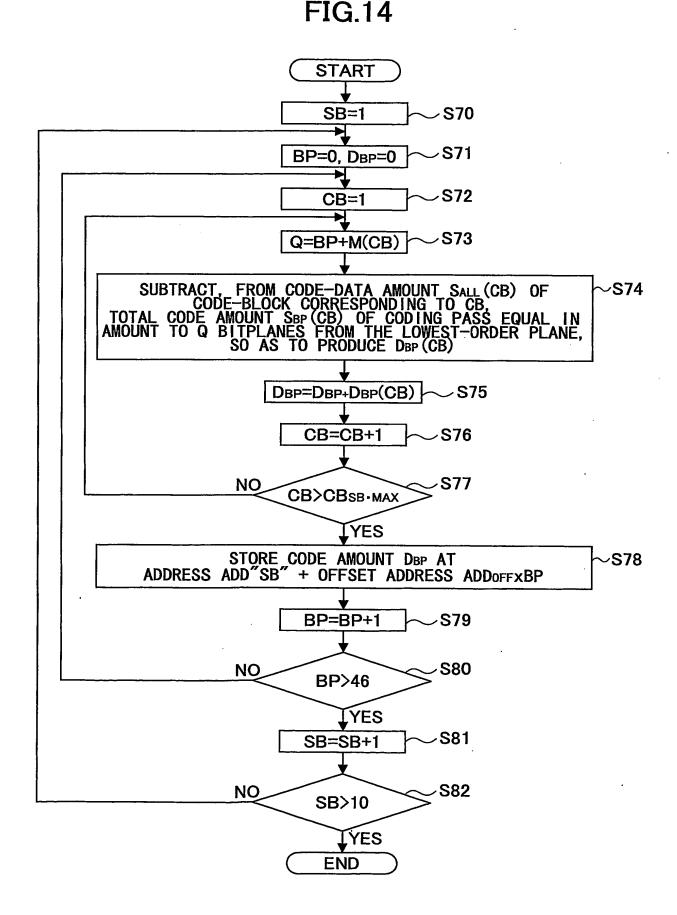
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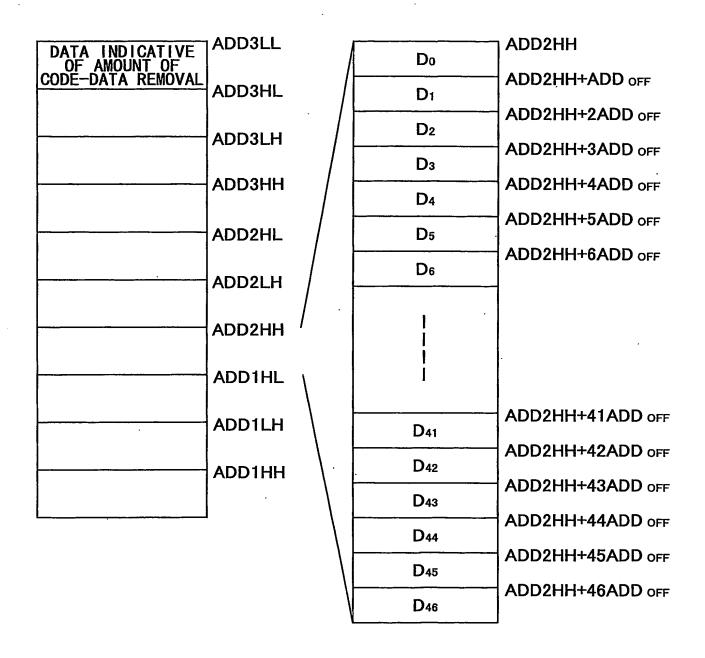
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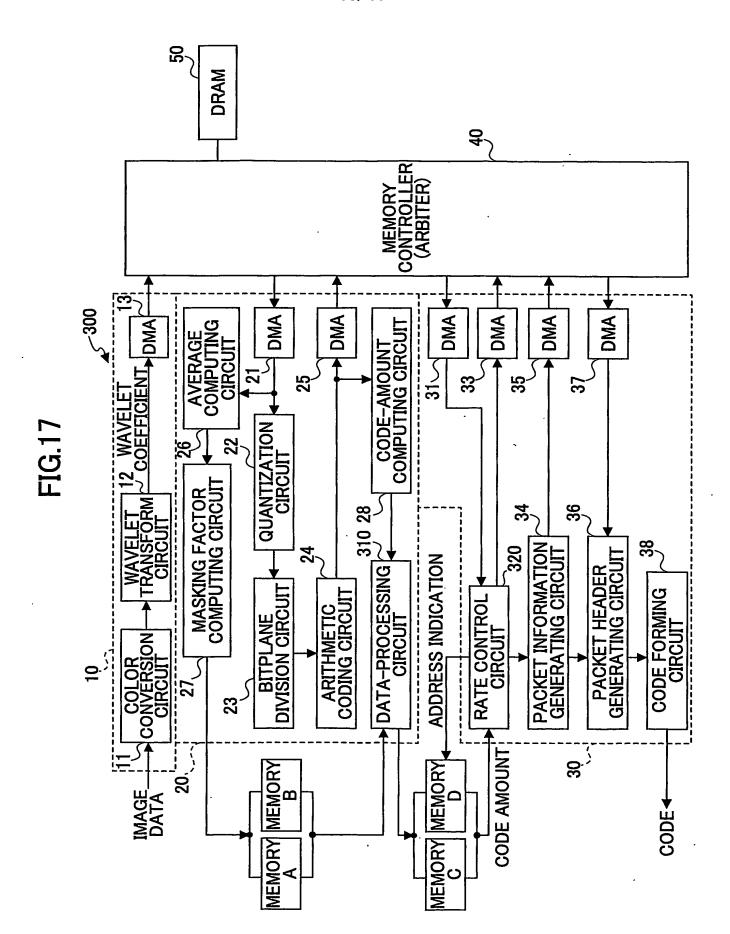
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3LL 3HL 3LH 3HH 2HL 2LH 2HH 1HL 1LH 1HH ADDRESS GENERATING CIRCUIT 230 **SELECTOR** TO PACKET INFORMATION GENERATING CIRCUIT FIG.16 ADD 3LL ADD 3HL ADD 3LH ADD 3HH ADD 2HL ADD 2LH ADD 2HH ADD 1HL ADD 1LH ADD 1HH 250

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17/18 FIG.18

